PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H03C 3/09 — A1

(11) International Publication Number: WO 95/16304

(43) International Publication Date: 15 June 1995 (15.06.95)

(21) International Application Number: PCT/US94/08998

(22) International Filing Date: 18 August 1994 (18.08.94)

(30) Priority Data:
08/163,671 7 December 1993 (07.12.93) US

(71) Applicant: NATIONAL SEMICONDUCTOR CORPORATION [US/US]; M/S 16-135, 1090 Kifer Road, Sunnyvale, CA 95086-3737 (US).

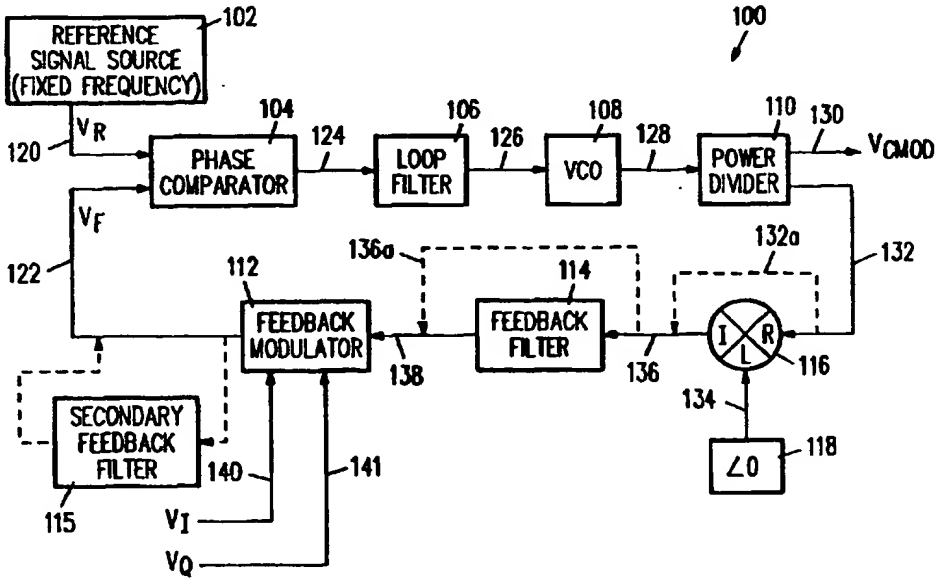
(72) Inventors: MADSEN, Benny; 3480 Granada Avenue, Santa Clara, CA 95051 (US). UMSTATTD, Ruth, E.; 3383 Victoria Avenue, Santa Clara, CA 95051 (US).

(74) Agent: RODDY, Richard, J.; National Semiconductor Corporation, M/S 16-135, 1090 Kifer Road, Sunnyvale, CA 94086-3737 (US).

(81) Designated States: JP, KR, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

(54) Title: PHASE/FREQUENCY MODULATOR



(57) Abstract

A modulator circuit for modulating a radio frequency (RF) signal with two signals which are in quadrature with one another includes a phase-locked loop (PLL) with a quadrature modulator within its output signal feedback path. The PLL generates an RF carrier signal which is phase-locked to a fixed-frequency reference signal and is modulated by modulating the VCO output feedback signal fed back to the phase detector of the PLL.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	**GB**	United Kingdom	**MR**	Mauritania
AU	Australia	**GE**	Georgia	**MW**	Malawi
BB	Barbados	**GN**	Guinea	**NE**	Niger
BE	Belgium	**GR**	Greece	**NL**	Netherlands
BF	Burkina Faso	**HU**	Hungary	**NO**	Norway
BG	Bulgaria	**IE**	Ireland	**NZ**	New Zealand
BJ	Benin	**IT**	Italy	**PL**	Poland
BR	Brazil	**JP**	Japan	**PT**	Portugal
BY	Belarus	**KE**	Kenya	**RO**	Romania
CA	Canada	**KG**	Kyrgystan	**RU**	Russian Federation
CF	Central African Republic	**KP**	Democratic People's Republic of Korea	**SD**	Sudan
CG	Congo			**SE**	Sweden
CH	Switzerland	**KR**	Republic of Korea	**SI**	Slovenia
CI	Côte d'Ivoire	**KZ**	Kazakhstan	**SK**	Slovakia
CM	Cameroon	**LI**	Liechtenstein	**SN**	Senegal
CN	China	**LK**	Sri Lanka	**TD**	Chad
CS	Czechoslovakia	**LU**	Luxembourg	**TG**	Togo
CZ	Czech Republic	**LV**	Latvia	**TJ**	Tajikistan
DE	Germany	**MC**	Monaco	**TT**	Trinidad and Tobago
DK	Denmark	**MD**	Republic of Moldova	**UA**	Ukraine
ES	Spain	**MG**	Madagascar	**US**	United States of America
FI	Finland	**ML**	Mali	**UZ**	Uzbekistan
FR	France	**MN**	Mongolia	**VN**	Viet Nam
GA	Gabon				

PHASE/FREQUENCY MODULATOR

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to phase/frequency modulation, and in particular, to phase/frequency modulation of a carrier signal generated within a phase-locked loop (PLL).

2. Description of the Related Art

Phase/frequency modulation, one of several techniques used for transmitting voice and data, is well known in the art, as are a number of phase/frequency modulator circuits and methods. The simplest technique for phase/frequency modulation is direct modulation of a voltage-controlled oscillator (VCO), as shown in Figure 1. The modulating signal directly controls the phase/frequency of the carrier signal generated by the VCO, thereby producing a phase/frequency-modulated carrier. While this technique is perhaps the simplest, it does have some drawbacks, perhaps the most important being that the accuracy and stability of the carrier frequency are determined solely by the VCO components.

One technique which has been used to ensure the accuracy and stability of the carrier frequency is to use a PLL, as shown in Figure 2. With this technique, the carrier signal generated by the VCO is phase-locked to a reference oscillator signal (typically stabilized and/or controlled by a crystal). Thus, with no modulation signal input, the carrier frequency of the output signal is accurate and stable. The modulating signal is summed with the VCO frequency control signal generated by the PLL. However, although this technique improves the accuracy and stability of the carrier frequency, a new problem is introduced with respect to the modulating signal input. Due to the phase-locking action of the PLL, frequencies within the modulating signal input which are outside the bandwidth of the loop filter are severely attenuated, if not virtually eliminated.

A modulator circuit which addresses these problems is shown in Figure 3. A quadrature modulator circuit is used to modulate a carrier signal generated by a PLL. A quadrature modulating signal, consisting of in-phase I and quadrature Q signals, or components, is used to modulate, e.g. quadrature-phase-shift-key (QPSK), the carrier signal from the PLL. Since the carrier signal is generated by a PLL, its frequency is accurate and stable, and since the modulating signal input is not affected by the loop filter of a PLL, its frequency content remains intact. However, this circuit has its own drawbacks, including difficulty in establishing and maintaining a high output signal-to-noise ratio (SNR) in the modulated carrier signal.

Figure 4 illustrates a modulator circuit which has been used as an attempt to solve the above-noted problems. As can be seen, this modulator includes some of the above-described modulator design elements, such as a PLL and quadrature modulator. The PLL is used, as discussed above, to provide for an accurate and stable carrier frequency. The quadrature modulator is used to modulate the reference signal for the PLL. This avoids attenuation of modulating signal frequencies by the loop filter, since the carrier signal generated by the VCO tracks the modulated reference signal. However, this circuit too has problems.

One problem concerns the in-phase I and quadrature Q signals, which are typically filtered digital signals representing binary data. As shown in Figure 5, the phase comparator typically consists of a phase detector with two dividers, e.g. counters, at its inputs. These dividers divide down the frequencies of the modulated reference and feedback signals by reference and feedback divisors R and N, respectively. These divisors R and N can each be preselected as virtually any integer. However, if these divisors R and N are not selected to be equal to one another, and the output frequency deviation of the modulated carrier

signal must equal the input frequency deviation of the modulating signal, then standard I and Q signals cannot be used to modulate the reference signal. In other words, if R≠N, then otherwise standard I and Q signals (whose relative amplitudes and frequencies are intended to determine the phase and frequency modulation, respectively, of the carrier signal) must be modified, e.g. prescaled in amplitude and/or frequency. Accordingly, the divisors R and N must be equal (i.e. R/N=1).

However, this requirement that R=N, in turn, introduces further complications. If the center frequency of the modulated carrier signal is high, then the frequency of the reference oscillator signal must also be high. This can be problematic, since the frequency of the reference oscillator signal is typically that of a clock or reference signal used elsewhere in the system and is usually much less than the center frequency of the modulated carrier signal. This can be partially solved by frequency down converting the output feedback signal within the PLL (as represented with the mixer, PLL and dashed line connection shown in Figure 4). However, there are limits to how low the frequency of the feedback signal inputted to the phase comparator can be. For example, the center frequency of the feedback signal must not be so low and/or the feedback divider's divisor N (Figure 5) must not be so high that the performance of the phase detector is adversely affected or that the bandwidth of the modulated carrier output from the PLL is unduly limited.

SUMMARY OF THE INVENTION

A signal modulator in accordance with the present invention includes a phase comparator and feedback modulator. The phase comparator receives a reference signal and a feedback signal, compares their signal phases and in accordance therewith generates a frequency control signal. The feedback modulator receives a carrier signal which has been generated in accordance with the frequency control signal, and also receives at least one modulation signal with which it modulates the carrier signal. The feedback modulator provides the modulated carrier signal as the feedback signal to the phase comparator.

In a preferred embodiment of the present invention, the phase comparator and feedback modulator form part of a PLL. The feedback modulator is a quadrature signal modulator which receives in-phase I and quadrature Q modulating signals. The phase comparator compares the reference and modulated feedback signal phases and generates a frequency control signal which is used to modulate a signal generator, such as a VCO. The initial modulation of the signal generator output is subsequently cancelled by feeding it back to the feedback modulator which "remodulates" it with the same I and Q modulating signals. This initial modulation and cancellation by subsequent "remodulation" is repeated with each later application of new I and Q modulation signals.

These and other features of the present invention will be understood upon consideration of the following detailed description of the invention and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a conventional technique used for generating a phase/frequency-modulated signal.

Figure 2 is a block diagram of a conventional PLL circuit used for generating a phase/frequency-modulated signal.

Figure 3 is a block diagram of a conventional quadrature modulator circuit.

Figure 4 is a block diagram of a conventional circuit used for generating a phase/frequency-modulated signal with a PLL and quadrature modulator.

Figure 5 is a block diagram of the phase comparator of Figure 4.

Figure 6 is a block diagram of a PLL circuit with a modulator in accordance with a preferred embodiment of the present invention.

Figure 7 is a block diagram of the phase comparator of Figure 6.

Figure 8 is a schematic diagram of the loop filter of Figure 6.

Figure 9 is a block diagram of the feedback modulator of Figure 6.

Figure 10 is a block diagram of an integrated circuit which includes a modulator in accordance with a preferred embodiment of the present invention.

Figure 11 is a block diagram of a transceiver system which uses the integrated circuit of Figure 10.

DETAILED DESCRIPTION OF THE INVENTION

Referring to Figure 6, a PLL circuit 100 with a modulator in accordance with the present invention includes: a reference signal source 102; a phase comparator 104; a loop filter 106; a VCO 108; a power divider 110; a feedback modulator 112; a feedback filter 114; a mixer 116; and a local oscillator signal source 118; all connected substantially as shown.

The reference signal source 102, e.g. a fixed frequency, crystal-controlled oscillator, provides a stable reference signal 120 to the phase comparator 104. The phase comparator 104 compares the phase of the reference signal 120 with the phase of a feedback signal 122 (discussed further below) and outputs a phase comparison signal 124, the amplitude of which represents the phase difference between the reference 120 and feedback 122 signals. This phase comparison signal 124 is lowpass filtered by the loop filter 106. The filtered phase comparison signal 126 is used as a frequency control, or tuning, signal for the VCO 108. The carrier signal 128 generated by the VCO 108 is divided in amplitude into two similar signals 130, 132 by the power divider 110. The first signal 130 is outputted as the modulated carrier signal, and the second signal 132 is used as the feedback signal for the PLL circuit 100.

The modulated feedback signal 132 is frequency down converted by the mixer 116, using a frequency conversion signal 134 from the local oscillator signal source 118. The frequency down converted, modulated feedback signal 136 is lowpass filtered by the feedback filter 114, which has a cutoff frequency selected to filter out any unwanted frequency conversion products produced within the mixer 116, as well as any artifacts of the modulated feedback signal 132 and/or frequency conversion signal 134 which may leak through the mixer 116.

The resulting feedback signal 138 is "remodulated" (discussed in more detail below) in the feedback modulator 112 by in-phase I (V_I) 140 and quadrature Q (V_Q) 141 modulation signals as they are introduced. The resulting "remodulated" feedback signal 122 is then used by the phase comparator 104, as discussed above. (Depending upon the application, a secondary feedback filter 115 can be used to provide additional filtering as needed.)

The "remodulation" of the frequency down converted and filtered feedback signal 138 to produce the "remodulated" feedback signal 122 can be described as follows. Initially, as modulation is introduced onto the input signal 138 by the feedback modulator 112 with the I 140 and Q 141 modulation signals, the VCO 108 provides a modulated output carrier signal 128. This modulated signal 128 is opposite in phase (-180 degrees) from the I 140 and Q 141 modulation signals and is quickly fed back (due to the relatively wide PLL loop bandwidth as established primarily by the loop filter 106) to the feedback modulator 112 (via the power divider 110, mixer 116 and filter 114). Hence, when the initially modulated feedback signal 138 is received by the feedback modulator 112, the "remodulation" thereof by the I 140 and Q 141 modulation signals cancels out such initial modulation. This initial modulation and almost immediate

cancellation by "remodulation" is repeated with each subsequent application of new, i.e. different, I 140 and Q 141 modulation signals.

Another way to consider this modulation technique is as follows. If viewed in the time domain (e.g. with an oscilloscope), the initially modulated feedback signal 122 from the feedback modulator 112 differs in frequency and/or phase from the reference signal 120; but this frequency and/or phase difference is quickly cancelled as described above. However, if viewed in the frequency domain (e.g. with a spectrum analyzer), the feedback signal 122 from the feedback modulator 112 appears to be a virtually continuous wave (CW) signal.

As should be recognized, depending upon the frequency range of operation and desired system performance, the frequency down conversion provided by the mixer 116 may be considered unnecessary or undesirable. Accordingly, the feedback signal 132a from the power divider 110 can be provided directly to the feedback filter 114. Further, if no frequency down conversion is used, the feedback filter 114 may not be necessary. Accordingly, a more direct connection 136a bypassing the filter 114 can be used, thereby providing the feedback signal 132a/136a from the power divider 110 directly to the feedback modulator 112.

Referring to Figure 7, a phase comparator 104 for a modulator in accordance with a preferred embodiment of the present invention includes reference 142 and feedback 144 signal dividers (i.e. counters), a phase detector 146 and a charge pump 147, all connected substantially as shown. The reference signal 120 frequency is divided down by a reference divisor R, and the feedback signal 122 frequency is divided down by a feedback divisor N. The phase difference between the divided-down reference 148 and divided-down feedback 150 signals is detected by the phase detector 146. A signal 151 (e.g. voltage or current) representing this phase difference is applied to the charge pump 147, which in turn, provides an output 124 (e.g. voltage or current) whose amplitude represents this phase difference. (A phase detector 146 used in a preferred embodiment of the present invention has a gain of approximately 4.0 milliamperes (mA) per 2π radians (360 degrees) of phase difference.)

A phase detector 146 and charge pump 147 which can be used in a modulator in accordance with the present invention are described in commonly assigned, co-pending U.S. patent application Serial No. 08/003,928, which is entitled "CHARGE PUMP CIRCUIT" and was filed on January 13, 1993, the disclosure of which is incorporated herein by reference.

Referring to Figure 8, a loop filter 106 for a PLL circuit 100 with a modulator in accordance with a preferred embodiment of the present invention is shown in schematic form. The lowpass filter function for this loop filter 106 design is based upon a VCO 108 having an input equivalent capacitance of approximately 66 picofarad (pF) and a VCO constant of approximately 27.27 megahertz per volt (MHz/V).

Referring to Figure 9, the feedback modulator 112 of Figure 6 includes a power divider 152, two mixers 154, 156, a quadrature (–90 degree) phase shifter 158, and a signal adder 162, all connected substantially as shown.

The power divider 152 receives the filtered feedback signal 138 and divides it in amplitude into two similar signals 164, 166. The first signal 164 is used as the "local oscillator" signal for the in-phase mixer 154. The second signal 166 is delayed in phase by 90 degrees by the phase shifter 158 prior to being used as the "local oscillator" signal for the quadrature mixer 156. The in-phase mixer 154 receives the in-phase modulation signal 140 and the quadrature mixer 156 receives the quadrature modulation signal 141. The in-phase 174 and quadrature 176 modulated outputs from the mixers 154, 156 are then summed by the adder 162 to produce the feedback signal 122 for use by the phase comparator 104, as discussed above (Figure 6).

Referring to Figure 10, an integrated circuit 1000 has been developed by the Assignee which includes the phase comparator 104 elements (Figure 7), feedback mixer 116 (Figure 6) and feedback

modulator 112 discussed above. This integrated circuit 1000 also includes a phase comparator circuit for a receiver circuit, as well as some additional control circuitry. Two external filter connections 1002, 1004 are provided for shunt lowpass filter elements, e.g. series RC networks. (The first external filter connection 1002 would be for the [primary] feedback filter 114, while the second connection 1004 would be for the secondary feedback filter 115.)

Referring to Figure 11, a transceiver system has been developed by the Assignee which incorporates the integrated circuit 1000 of Figure 10.

An implementation of a PLL circuit 100 with a modulator in accordance with the foregoing discussion (Figures 6–10) was constructed for test purposes in which: the reference signal 120 frequency was 960 MHz (as was the center frequency of the feedback signal 122); the reference R and feedback N divider divisors were 192 and 20, respectively; the VCO carrier 128 frequency was 910 MHz; the frequency conversion signal 134 frequency was 810 MHz; the cutoff frequency of the loop filter 106 was approximately 400 KHz; and the cutoff frequency of the feedback filter 114 was approximately 500 MHz.

As can be seen from the foregoing, a modulator in accordance with the present invention provides several advantages over the prior art: standard in–phase I and quadrature Q modulation signals can be used; the wideband noise floor, determined by the performance of the VCO, is typically better than that available with conventional quadrature modulators alone (i.e. without lossy filtering); the output carrier frequency deviation is equal to that of the frequency deviation of the baseband modulating signal; the PLL divider's divisors are low, thereby reducing the gain associated with the inband noise floor plus allowing for fast phase and/or frequency tuning or switching by the PLL; no modulation of the reference signal is required; the frequency of the PLL reference signal can be chosen arbitrarily; frequency pulling or pushing of the VCO output (e.g. due to output load changes, dc power spikes or interference [e.g. RFI]) is suppressed, or compensated for, very quickly; and the modulated output signal has a constant amplitude envelope since it comes directly from a VCO rather than directly from a quadrature modulator, thereby providing a more optimal drive signal for a nonlinear (e.g. class C) power amplifier.

Various other modifications and alterations in the structure and method of operation of this invention will be apparent to those skilled in the art without departing from the scope and spirit of this invention. Although the invention has been described in connection with specific preferred embodiments, it should be understood that the invention as claimed should not be unduly limited to such specific embodiments.

WHAT IS CLAIMED IS:

1. A signal modulator comprising:

phase comparator means for receiving a reference signal with an associated reference signal phase, receiving a feedback signal with an associated feedback signal phase, comparing said reference and feedback signal phases, and in accordance therewith generating a frequency control signal; and

feedback modulator means, coupled to said phase comparator means, for receiving a carrier signal generated in accordance with said frequency control signal, receiving at least one modulation signal, modulating said received carrier signal with said at least one modulation signal to produce a modulated carrier signal, and outputting said modulated carrier signal as said feedback signal.

2. A signal modulator as recited in Claim 1, wherein said phase comparator means comprises phase detector means for detecting a phase difference between said reference and feedback signal phases, and in accordance therewith outputting a phase difference signal corresponding to said phase difference.

3. A signal modulator as recited in Claim 1, wherein said feedback modulator means comprises a quadrature signal modulator and said at least one modulation signal comprises a plurality of quadrature signals.

4. A signal modulator as recited in Claim 1, further comprising loop filter means, coupled to said phase comparator means, for receiving and filtering said frequency control signal.

5. A signal modulator as recited in Claim 1, further comprising feedback filter means, coupled to said feedback modulator means, for receiving and filtering said carrier signal prior to said reception and modulation thereof by said feedback modulator means.

6. A signal modulator as recited in Claim 5, further comprising frequency converter means, coupled to said feedback filter means, for receiving and frequency converting said carrier signal prior to said reception and filtering thereof by said feedback filter means.

7. A signal modulator as recited in Claim 6, wherein said frequency converter means comprises a mixer.

8. A signal modulator as recited in Claim 1, further comprising frequency converter means, coupled to said feedback modulator means, for receiving and frequency converting said carrier signal prior to said reception and modulation thereof by said feedback modulator means.

9. A signal modulator as recited in Claim 8, wherein said frequency converter means comprises a mixer.

10. A signal modulator as recited in Claim 8, further comprising signal generator means, coupled to said phase comparator means and said feedback modulator means, for receiving said frequency control signal and in accordance therewith generating said carrier signal.

11. A signal modulator as recited in Claim 10, wherein said signal generator means comprises a voltage-controlled oscillator (VCO) and said frequency control signal comprises a voltage signal.

12. A signal modulator as recited in Claim 1, further comprising signal generator means, coupled to said phase comparator means and said feedback modulator means, for receiving said frequency control signal and in accordance therewith generating said carrier signal.

13. A signal modulator as recited in Claim 12, wherein said signal generator means comprises a voltage-controlled oscillator (VCO) and said frequency control signal comprises a voltage signal.

14. A signal modulator comprising:

a phase comparator which receives a reference signal with an associated reference signal phase, receives a feedback signal with an associated feedback signal phase, compares said reference and feedback signal phases, and in accordance therewith generates a frequency control signal; and

a feedback modulator, coupled to said phase comparator, which receives a carrier signal generated in accordance with said frequency control signal, receives at least one modulation signal, modulates said received carrier signal with said at least one modulation signal to produce a modulated carrier signal, and outputs said modulated carrier signal as said feedback signal.

15. A signal modulator as recited in Claim 14, wherein said phase comparator comprises a phase detector which detects a phase difference between said reference and feedback signal phases, and in accordance therewith outputs a phase difference signal corresponding to said phase difference.

16. A signal modulator as recited in Claim 14, wherein said feedback modulator comprises a quadrature signal modulator and said at least one modulation signal comprises a plurality of quadrature signals.

17. A signal modulator as recited in Claim 14, further comprising a loop filter, coupled to said phase comparator, which receives and filters said frequency control signal.

18. A signal modulator as recited in Claim 14, further comprising a feedback filter, coupled to said feedback modulator, which receives and filters said carrier signal prior to said reception and modulation thereof by said feedback modulator.

19. A signal modulator as recited in Claim 18, further comprising a frequency converter, coupled to said feedback filter, which receives and frequency converts said carrier signal prior to said reception and filtering thereof by said feedback filter.

20. A signal modulator as recited in Claim 19, wherein said frequency converter comprises a mixer.

21. A signal modulator as recited in Claim 14, further comprising a frequency converter, coupled to said feedback modulator, which receives and frequency converts said carrier signal prior to said reception and modulation thereof by said feedback modulator.

22. A signal modulator as recited in Claim 21, wherein said frequency converter comprises a mixer.

23. A signal modulator as recited in Claim 21, further comprising a signal generator, coupled to said phase comparator and said feedback modulator, which receives said frequency control signal and in accordance therewith generates said carrier signal.

24. A signal modulator as recited in Claim 23, wherein said signal generator comprises a voltage-controlled oscillator (VCO) and said frequency control signal comprises a voltage signal.

25. A signal modulator as recited in Claim 14, further comprising a signal generator, coupled to said phase comparator and said feedback modulator, which receives said frequency control signal and in accordance therewith generates said carrier signal.

26. A signal modulator as recited in Claim 25, wherein said signal generator comprises a voltage-controlled oscillator (VCO) and said frequency control signal comprises a voltage signal.

27. A signal modulation method comprising the steps of:

receiving a reference signal with an associated reference signal phase;

receiving a feedback signal with an associated feedback signal phase;

comparing said reference and feedback signal phases and in accordance therewith generating a frequency control signal;

receiving a carrier signal generated in accordance with said frequency control signal;

receiving at least one modulation signal;

modulating said received carrier signal with said at least one modulation signal to produce a modulated carrier signal; and

outputting said modulated carrier signal as said feedback signal.

28. A signal modulation method as recited in Claim 27, wherein said step of comparing said reference and feedback signal phases and in accordance therewith generating a frequency control signal comprises detecting a phase difference between said reference and feedback signal phases and in accordance therewith outputting a phase difference signal corresponding to said phase difference.

29. A signal modulation method as recited in Claim 27, wherein said step of modulating said received carrier signal with said at least one modulation signal to produce a modulated carrier signal comprises quadrature modulating said received carrier signal with a plurality of quadrature signals.

30. A signal modulation method as recited in Claim 27, further comprising the step of filtering said frequency control signal.

31. A signal modulation method as recited in Claim 27, further comprising the step of filtering said carrier signal prior to said modulation thereof.

32. A signal modulation method as recited in Claim 31, further comprising the step of frequency converting said carrier signal prior to said filtering thereof.

33. A signal modulation method as recited in Claim 32, wherein said step of frequency converting said carrier signal prior to said filtering thereof comprises mixing said carrier signal with a frequency conversion signal.

34. A signal modulation method as recited in Claim 27, further comprising the step of frequency converting said carrier signal prior to said modulation thereof.

35. A signal modulation method as recited in Claim 34, wherein said step of frequency converting said carrier signal prior to said modulation thereof comprises mixing said carrier signal with a frequency conversion signal.

36. A signal modulation method as recited in Claim 34, further comprising the step of receiving said frequency control signal and in accordance therewith generating said carrier signal.

37. A signal modulation method as recited in Claim 36, wherein said step of receiving said frequency control signal and in accordance therewith generating said carrier signal comprises receiving a voltage signal and in accordance therewith generating said carrier signal with a voltage-controlled oscillator (VCO).

38. A signal modulation method as recited in Claim 27, further comprising the step of receiving said frequency control signal and in accordance therewith generating said carrier signal.

39. A signal modulation method as recited in Claim 38, wherein said step of receiving said frequency control signal and in accordance therewith generating said carrier signal comprises receiving a voltage signal and in accordance therewith generating said carrier signal with a voltage-controlled oscillator (VCO).

40. An integrated circuit which includes an internal signal modulator circuit comprising:

phase comparator means for receiving a reference signal with an associated reference signal phase, receiving a feedback signal with an associated feedback signal phase, comparing said reference and feedback signal phases, and in accordance therewith generating a frequency control signal; and

feedback modulator means, coupled to said phase comparator means, for receiving a carrier signal generated in accordance with said frequency control signal, receiving at least one modulation signal, modulating said received carrier signal with said at least one modulation signal to produce a modulated carrier signal, and outputting said modulated carrier signal as said feedback signal.

41. An integrated circuit as recited in Claim 40, wherein said phase comparator means comprises phase detector means for detecting a phase difference between said reference and feedback signal phases, and in accordance therewith outputting a phase difference signal corresponding to said phase difference.

42. An integrated circuit as recited in Claim 40, wherein said feedback modulator means comprises a quadrature signal modulator and said at least one modulation signal comprises a plurality of quadrature signals.

43. An integrated circuit as recited in Claim 40, further comprising frequency converter means for receiving and frequency converting said carrier signal prior to said reception and modulation thereof by said feedback modulator means.

44. An integrated circuit as recited in Claim 43, wherein said frequency converter means comprises a mixer.

45. An integrated circuit which includes an internal signal modulator circuit comprising:

a phase comparator which receives a reference signal with an associated reference signal phase, receives a feedback signal with an associated feedback signal phase, compares said reference and feedback signal phases, and in accordance therewith generates a frequency control signal; and

a feedback modulator, coupled to said phase comparator, which receives a carrier signal generated in accordance with said frequency control signal, receives at least one modulation signal, modulates said received carrier signal with said at least one modulation signal to produce a modulated carrier signal, and outputs said modulated carrier signal as said feedback signal.

46. An integrated circuit as recited in Claim 45, wherein said phase comparator comprises a phase detector which detects a phase difference between said reference and feedback signal phases, and in accordance therewith outputs a phase difference signal corresponding to said phase difference.

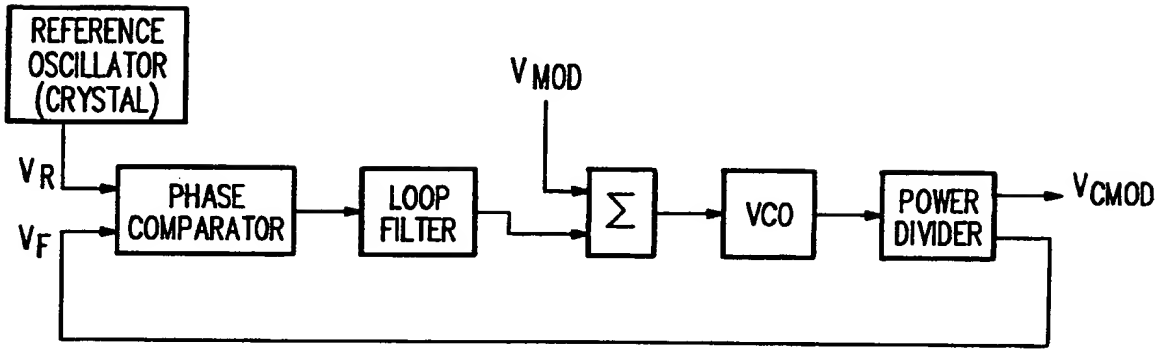
47. An integrated circuit as recited in Claim 45, wherein said feedback modulator comprises a quadrature signal modulator and said at least one modulation signal comprises a plurality of quadrature signals.

48. An integrated circuit as recited in Claim 45, further comprising a frequency converter which receives and frequency converts said carrier signal prior to said reception and modulation thereof by said feedback modulator.

49. An integrated circuit as recited in Claim 48, wherein said frequency converter comprises a mixer.

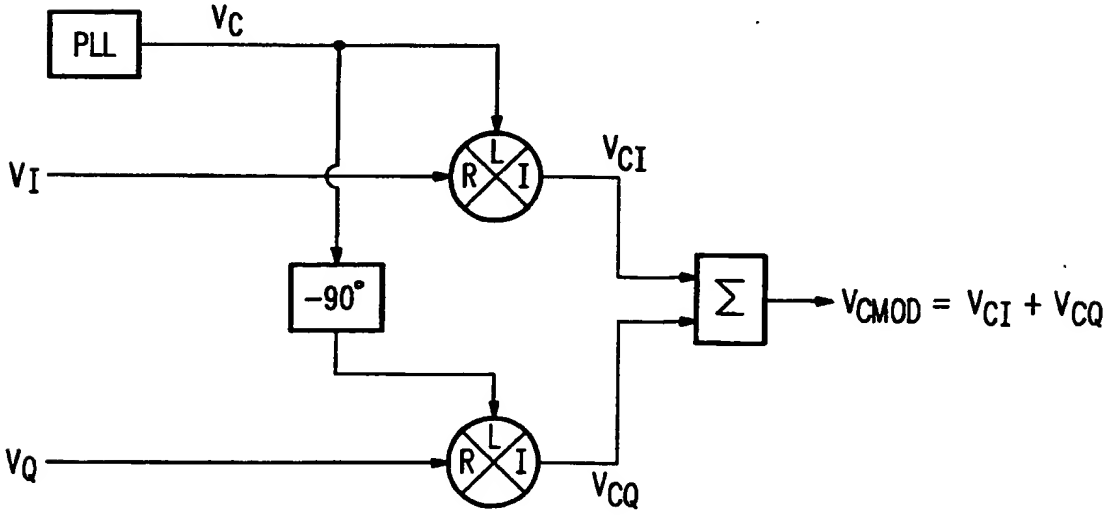
PRIOR ART

FIG. 1



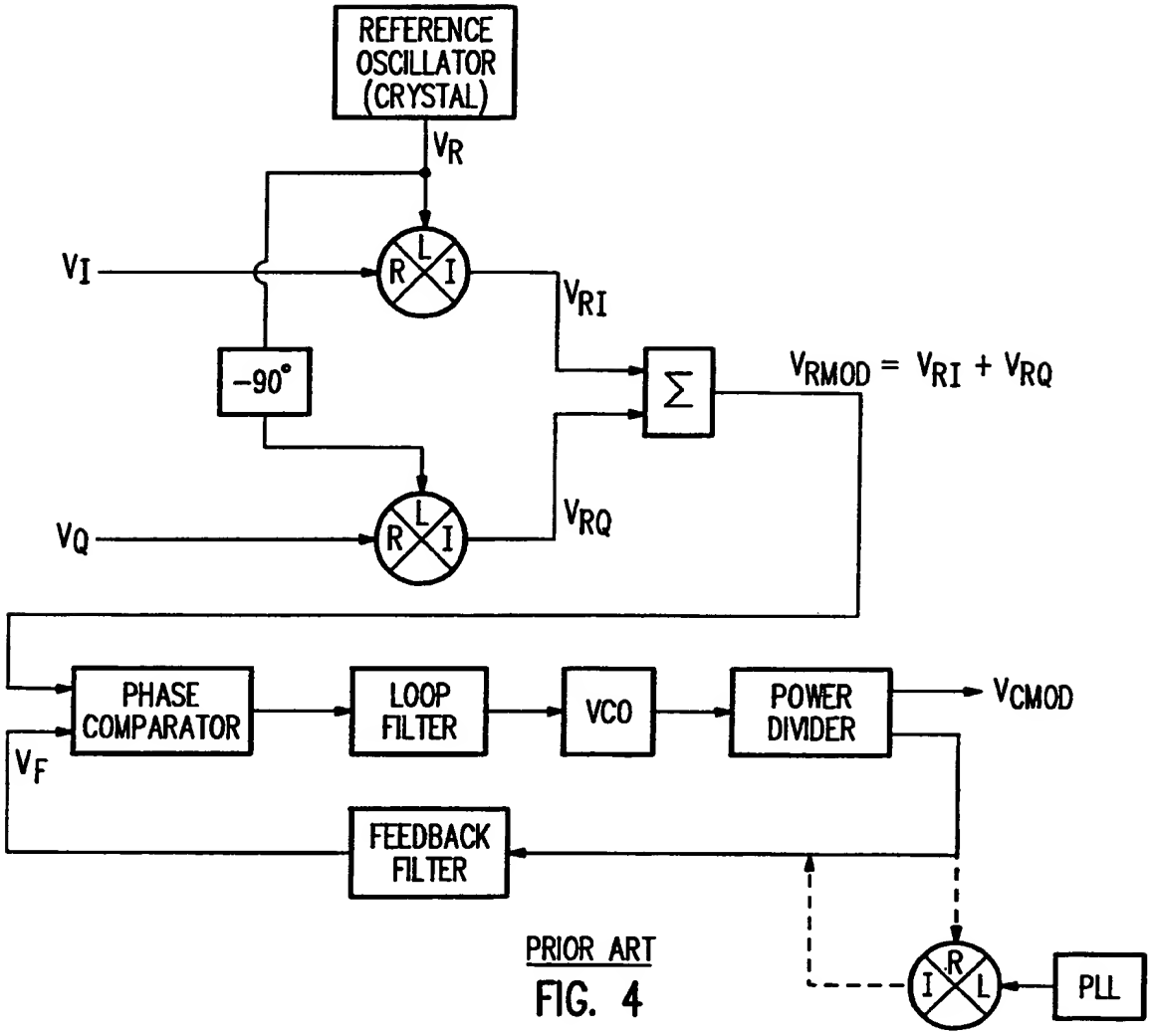
PRIOR ART

FIG. 2



PRIOR ART

FIG. 3



PRIOR ART

FIG. 4

PRIOR ART

FIG. 5

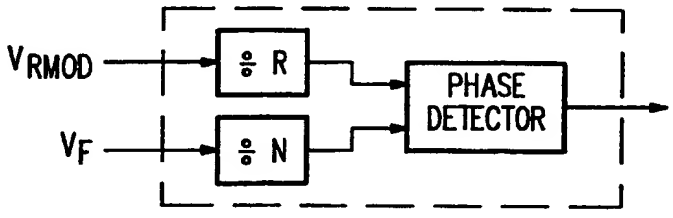
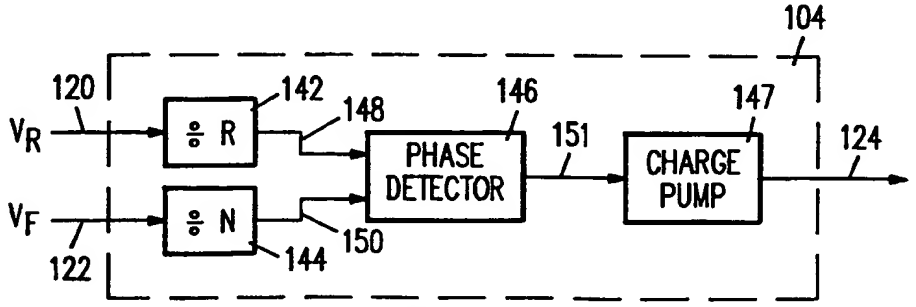


FIG. 7



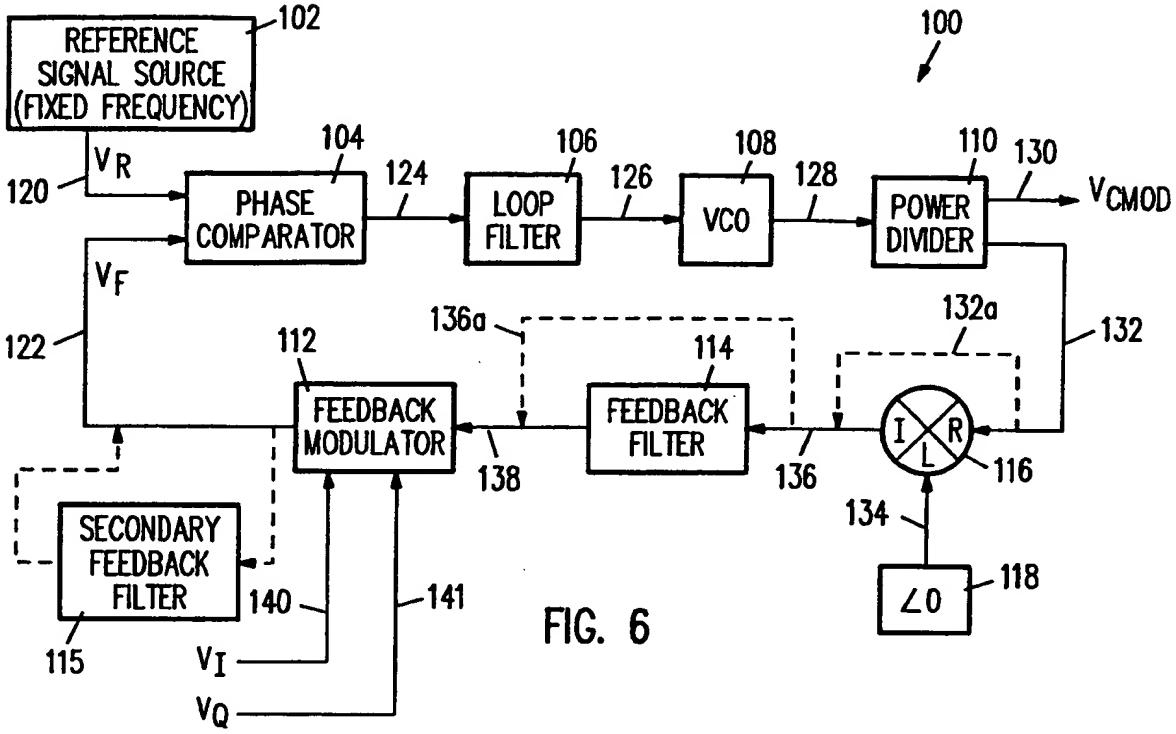


FIG. 6

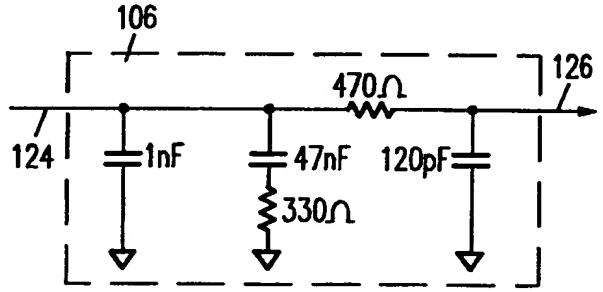


FIG. 8

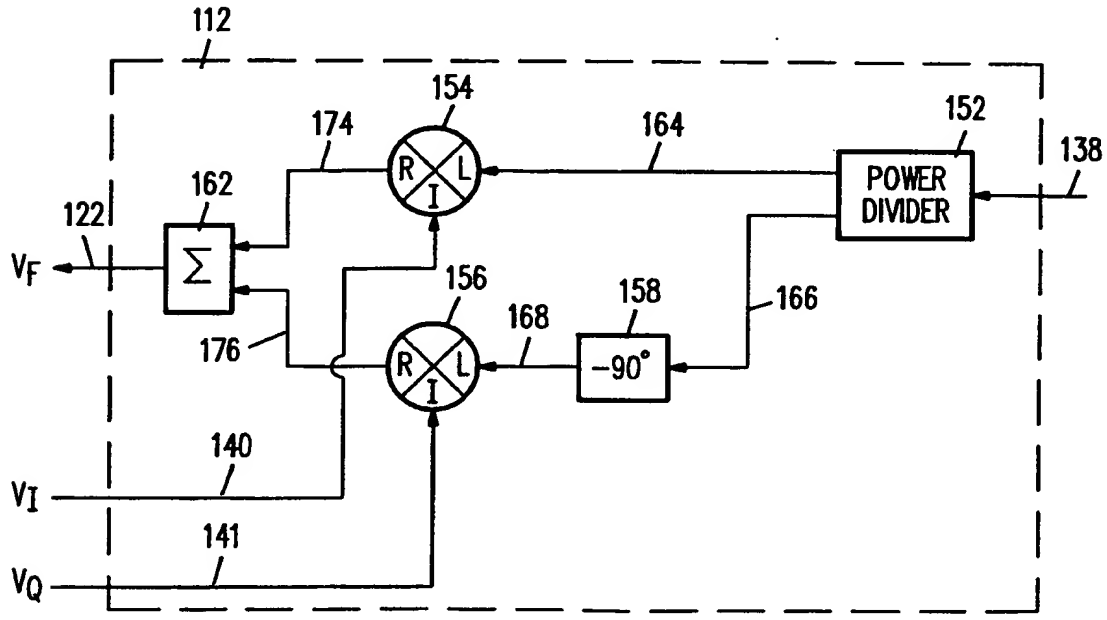


FIG. 9

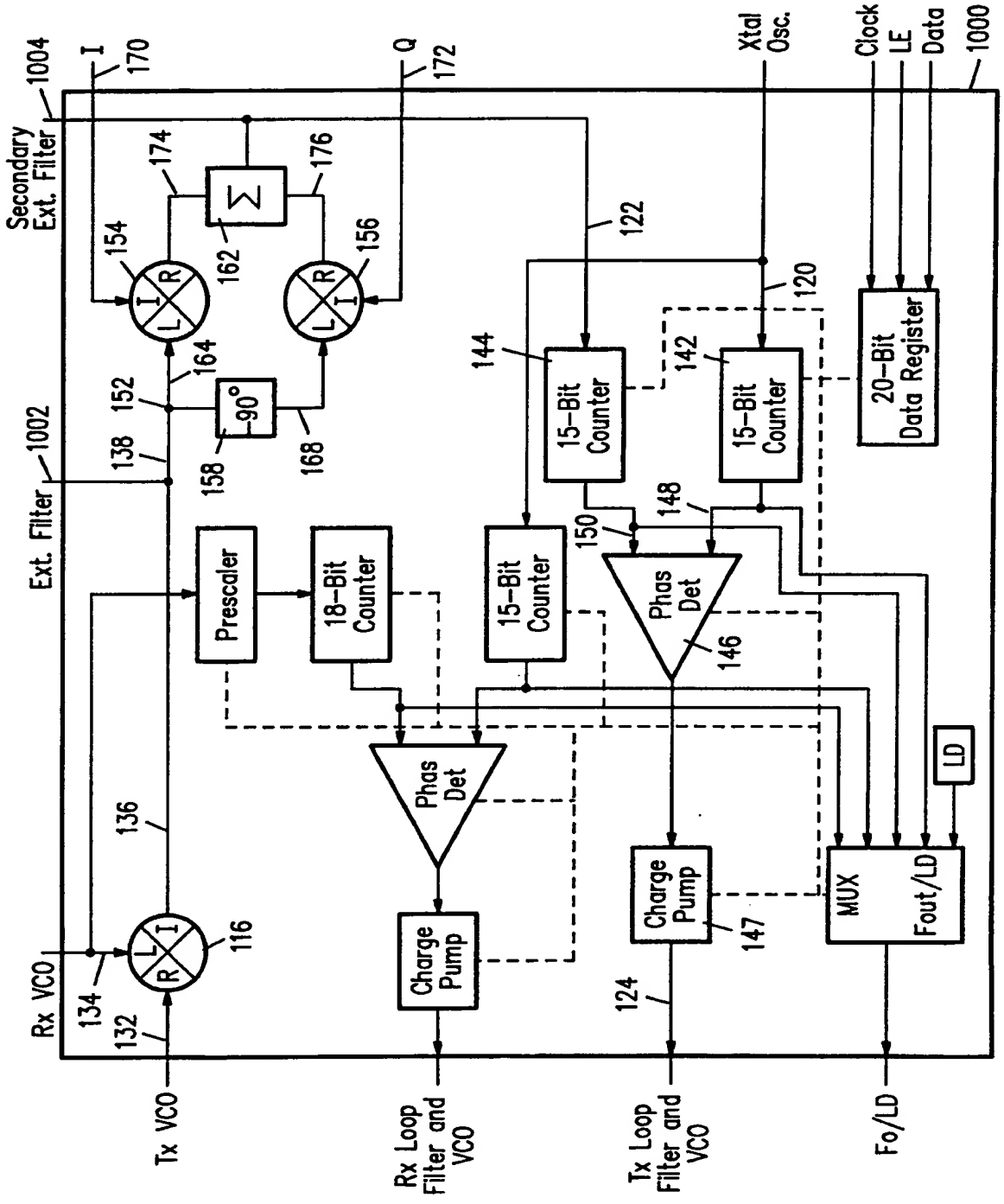

1004
I
170
Q
172
Xtal Osc.
Clock
LE
Data
1000
Secondary Ext. Filter
174
176
154
162
156
122
120
144
142
15-Bit Counter
15-Bit Counter
20-Bit Data Register
164
152
90°
1002
138
158
168
Ext. Filter
148
150
Prescaler
18-Bit Counter
15-Bit Counter
Phas Det
146
LD
Phas Det
136
Charge Pump
Charge Pump
MUX
Fout/LD
147
116
Rx VCO
134
132
124
Tx VCO
Rx Loop Filter and VCO
Tx Loop Filter and VCO
Fo/LD

FIG. 10

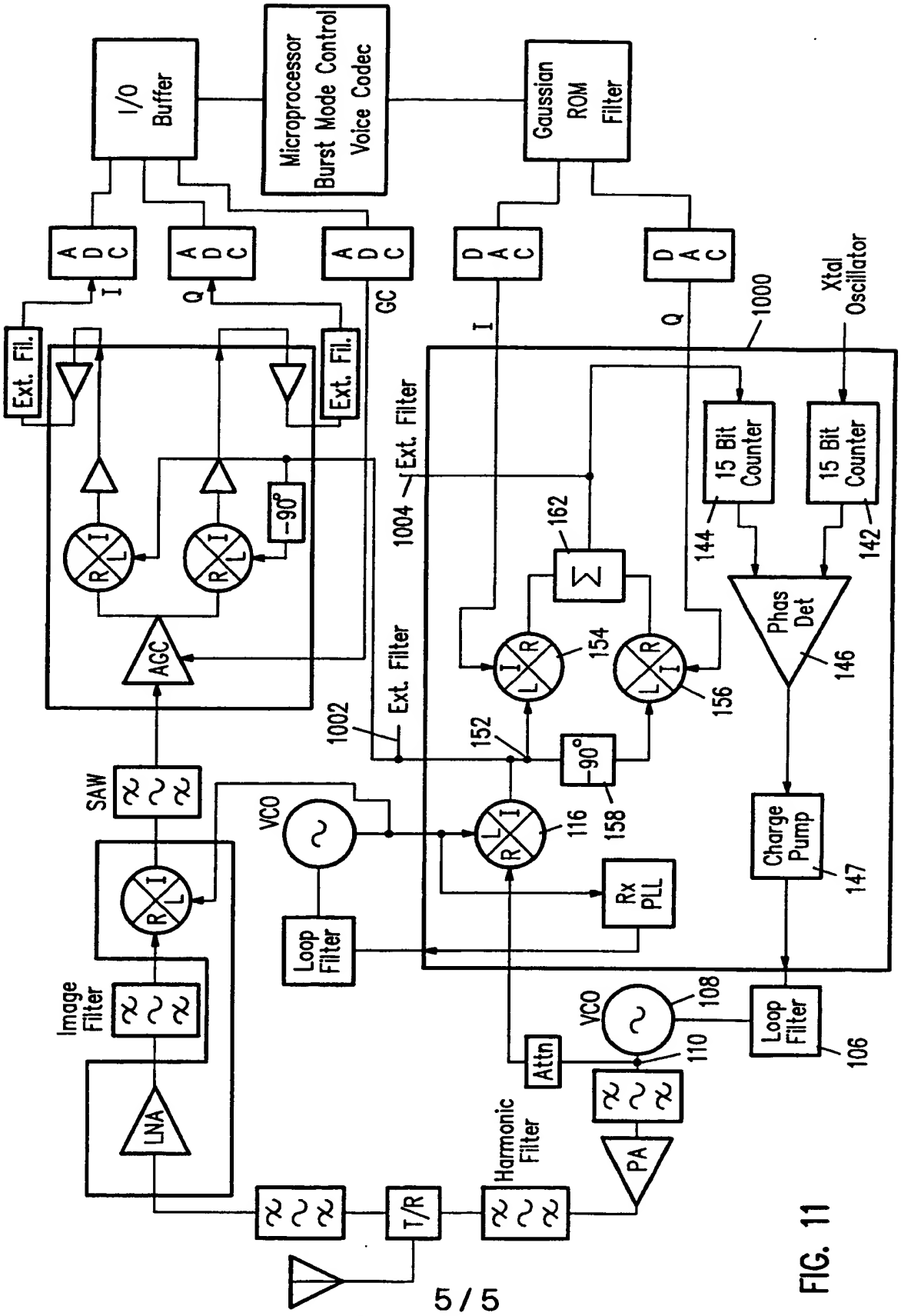

I/O Buffer
Microprocessor Burst Mode Control Voice Codec
Gaussian ROM Filter
A D C
D A C
I
Q
GC
Xtal Oscillator
1000
Ext. Fil.
Ext. Filter
1004
1002
15 Bit Counter
144
142
162
Phas Det
146
154
156
152
158
116
-90°
AGC
SAW
VCO
Loop Filter
Rx PLL
Charge Pump
147
Image Filter
LNA
Attn
108
110
106
Harmonic Filter
PA
T/R

FIG. 11

INTERNATIONAL SEARCH REPORT

Inter. Application No
PCT/US 94/08998

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H03C3/09

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H03C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US,A,4 021 757 (E.J. NOSSEN) 3 May 1977 see column 1, line 51 - column 6, line 19; figures 1-3	1-49
A	GB,A,2 260 044 (NOKIA MOBILE PHONES LIMITED) 31 March 1993 see abstract; figure	5-9, 18-22, 31-35
X	GB,A,1 161 206 (THE PLESSEY COMPANY LIMITED) 13 August 1969 see page 2, line 7 - line 67; figure	1-49

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 December 1994	10. 01. 95

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Dhondt, I

Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP,A,0 209 754 (MOTOROLA) 28 January 1987 see abstract; figure 7	1,2,4, 12-15, 17, 25-28, 30,38,39

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter. Application No
PCT/US 94/08998

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A-4021757	03-05-77	DE-A,B,C 2700429	13-10-77
		FR-A,B 2347820	04-11-77
		GB-A- 1570586	02-07-80
		JP-A- 52123857	18-10-77
GB-A-2260044	31-03-93	NONE	
GB-A-1161206	13-08-69	NONE	
EP-A-0209754	28-01-87	US-A- 4755774	05-07-88